1. **Course number and name**
   CptS 260: Introduction to Computer Architecture

2. **Credits and contact hours**
   3 credits, 3 lecture hours

3. **Instructor’s or course coordinator’s name**
   Zhe Dang

4. **Textbook, title, author, and year**

5. **Specific course information**
   a. **Catalog description:** Computer systems architecture; logic, data representation, assembly language, memory organization and trends.
   b. **Prerequisites or corequisites:** knowledge of structured programming languages such as C++/Java; Concurrent with CptS223.
   c. **Required, elective, or selected elective:** Required.

6. **Specific goals for the course**
   By the end of the course, students will be able to
   - Represent numbers in various bases, convert numbers from one basis to another, and perform arithmetic operations on the numbers (1e)
   - Apply floating point standard representations to convert floating point numbers from decimal to binary and vice versa (1e, 6b)
   - Apply the knowledge of computer performance to compute response time of a computer on a given program (1e)
   - Write MIPS assembly code for a given problem description
   - Write assembly code equivalence of a high-level problem given for example in C
   - Assess performance of two computers on a given program workload (2b)
   - Identify how computers execute instructions and how register and memory contents are modified as a result of this execution (1e)
   - Simplify a given Boolean function, draw its equivalent gate-level circuit, and compare the simplified circuit with the original one in terms of delay and area complexity (2b, 6b)
   - Identify values of various control signals in a computer as a program is being executed by CPU (1e)
   - Identify what hardware blocks are active during execution of various instructions (1e)
   - Apply the knowledge of pipelining to compute the amount of time that it takes to execute a program on a pipelined architecture (1e, 6a)
   - Assess performance of a pipelined architecture versus an architecture without pipelining (2b)
● Understand and apply strategies to deal with hazards in an architecture with pipelining (1e)
● Compare performance of a computer with cache memory versus one without cache memory (2b)
● Apply the knowledge of sequential circuits to identify how output of a sequential circuit changes during each clock cycle (1e, 6b)
● Identify content of a cache memory for various cache designs including direct mapped, set associative, and fully associative designs (1e)
● Apply the knowledge of memory hierarchy to compute hit rate, miss rate, and miss penalty for various memory hierarchy designs (1e, 6b)

7. Brief list of topics to be covered
   ● Introduction to Computer Architecture
   ● Computer Performance Analysis
   ● Integer Representation & Arithmetic
   ● Floating Point Representation & Arithmetic
   ● MIPS Assembly Programming
   ● Basics of Digital Design
   ● Single Cycle Simple MIPS Architecture
   ● Pipelining & Pipelined MIPS Architecture
   ● Memory Hierarchy & Cache Memory Design
   ● Current and Future Computers