

- 1. Course number and name**
EE 434: ASIC and Digital Systems Design
- 2. Credits and contact hours**
3 (three lecture hours per week)
- 3. Instructor's or course coordinator's name**
Dae Hyun Kim
- 4. Textbook, title, author, and year**
Wayne Wolf. 2004. *FPGA-Based System Design*. Prentice Hall.
Other supplemental materials
Instructor notes/slides will be provided for some topics.
- 5. Specific course information**
 - a. *Catalog description:* Application Specific Integrated Circuit and Digital System Design methods, semi-custom, full-custom, and field-programmable devices; digital system architectures, electronics, and tests.
 - b. *Prerequisites or corequisites:* E E 234 with a C or better; E E 321 with a C or better; certified major in Electrical Engineering, Computer Science, or Computer Engineering.
- 6. Specific goals for the course**

By the end of the course, students will be able to

 - Design and analyze combinational and sequential logic gates using NMOS and PMOS transistors (1, 2)
 - Explain full-custom, semi-custom, standard-cell-based, and array-based VLSI design methodologies (2)
 - Design and analyze VLSI layouts (placement, routing, power grid design, clock tree synthesis) using P&R software (1,2,6)
 - Explain compare the principles of FPGAs (1,2)
 - Design digital systems such as simple processors and network routers using HDLs and synthesize the systems (2,6)
 - Explain various design for testability techniques and apply them to real digital systems (1,6)
- 7. Brief list of topics to be covered**
 - CMOS circuit design methodologies, 6hrs
 - Implementation methods: Custom and semi-custom design, standard-cell-based design, array-based design, 3hrs
 - Placement and routing, power grid and clock design, 3hrs
 - Full-custom layout design, 3hrs
 - FPGA: Comparison between standard ASICs and FPGAs, different FPGA families, their advantages and disadvantages, 8hrs

- RTL design and synthesis: VHDL and Verilog, design of simple processors, network routers and other important digital blocks. Emphasis on synthesis, synthesis through scripts, use of Synopsys Design Compiler, 14hrs
- Design for Testability (DFT) techniques: Fault models, fault equivalence, BIST, LFSR, MISR, Scan design, JTAG, IDDQ test, SoC test, P1500, 8hrs

