1. **Course number and name**  
EE 334: Computer Architecture

2. **Credits and contact hours**  
3.0 (three lecture hours per week)

3. **Instructor’s or course coordinator’s name**  
José Delgado-Frias

4. **Text book, title, author, and year**  
*Other supplemental materials*  
Instructor notes/slides will be provided for some topics.

5. **Specific course information**  
a. **Catalog description:** Modern developments in digital system design, parallel structures, pipelining, input/output, high speed circuits, experience in digital system design; emphasis on CPU architecture.  
b. **Prerequisites or co-requisites:** EE 234 with a C or better; certified major in Electrical Engineering, Computer Science, or Computer Engineering.

6. **Specific goals for the course**  
At the end of this course, students must be able to:  
- Use metrics to assess the performance of a computer system (1b, 1c, 1d, 1e, 2c)  
- Determine the control requirements/lines for execution of specific instructions (1b, 1e)  
- Analyze performance and instruction throughput of single-cycle, multi-cycle, and pipelined implementations of an instruction set (1b, 1c, 1d, 1e, 2b)  
- Detect pipeline hazards and identify potential solutions to those hazards and evaluate them. (1a, 1b, 1c, 6a, 6b, 6c)  
- Identify cache design parameters and determine how they affect cache hit rate and performance (2b, 2c, 2e)  
- Map a virtual address into a physical address (6c)

7. **Brief list of topics to be covered**  
- Instruction set architecture,  
- Computer arithmetic, number representation, floating point numbers and arithmetic,  
- Processor datapath and single instruction,  
- Control signals,  
- Data hazards and forwarding technique,  
- Control (branch/jump) hazards,  
- Branch/jump prediction scheme to mitigate control hazards,  
- Instruction level parallelism,
- Memory Hierarchy and cache,
- Virtual memory.